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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/935,940	08/23/2001	William J. Huff	P04978 (NATI15-04978)	1426	
75	90 11/10/2004		EXAM	INER	
Docket Clerk P.O. Drawer 800889			JOSEPH, JAISON		
Dallas, TX 75			ART UNIT	PAPER NUMBER	
·			2634	2634	
			DATE MAILED: 11/10/2004		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	09/935,940	HUFF ET AL.				
Office Action Summary	Examiner	Art Unit				
	Jaison Joseph	2634				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be timed within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) ☐ Responsive to communication(s) filed on 23 At 2a) ☐ This action is FINAL. 2b) ☐ This 3) ☐ Since this application is in condition for allowar closed in accordance with the practice under Example 2.	action is non-final. nce except for formal matters, pro					
Disposition of Claims						
4) ☐ Claim(s) 1-10 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-10 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or	wn from consideration.	,				
Application Papers						
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) accomplicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Examine	epted or b) objected to by the I drawing(s) be held in abeyance. See ion is required if the drawing(s) is ob	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summary Paper No(s)/Mail Do 5) Notice of Informal F					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	6) Other:	atom Application (F 10-102)				

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 2 and 9 – 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Eriksson el at (US Patent 6,011,815).

Regarding Claims 1 and 9, Eriksson el at teaches that the output of the frequency modulator is connected to the delta sigma modulator. Eriksson teaches that on a FSK (frequency shift keyed) receiver (column 1 line 5-10) comprising a phase lock loop (PLL) having a phase detector and frequency divider circuit (column 5 line 17-19), which can adjust the frequency dividing factor depends on the input signal, a frequency discriminator that receives the incoming signal and generate a correction signal, and a delta-sigma modulator, controlled by the signal from the frequency detector, that controls the frequency divider circuit (column 5 line 48-49).

Regarding claims 2 and 10, with the limitations of claim 1 and 9 respectively, Eriksson el at teaches that channel selection can be performed by adding an offset to the input of the delta sigma modulator (column 2 line 26-28). This is equivalent to the limitation of subtracting the correction signal from the normal carrier frequency as recited in claims 2 and 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eriksson el at (US Patent 6,011,815) as applied to claim 1 above, and in view of Takahiro el at (US Patent 5,170,131).

Regarding claim 3, which inherits the limitations of the claim 1, Eriksson et al cited as explained above paragraph. Eriksson failed to teach that a frequency discriminator mixes the incoming signal and a reference signal to generate an intermediate frequency signal, and split the intermediate signal into two signals. However, Takahiro et al teach that a frequency discriminator comprises a mixer (figure 2 element 11) that receives an incoming signal (figure 2 element 10) and mixes with signal from local oscillator (figure 2 element 15) to generate an intermediate frequency signal (figure 2 signal I). It would have been obvious to an ordinary skilled in the art at the time of the invention to use Takahiro's frequency discriminator in place of Eriksson's frequency discriminator to benefit simpler design.

Regarding claim 4, which inherits the limitations of the claim 3, Takahiro et al teach that split the incoming signal 10 (see figure 1) into two and mix the split signal with signal from the local oscillator 15 in mixers 11 and 12 to generate intermediate signals I and Q respectively. It is well known in the art that splitting a signal into two and mixing with another signal in two mixers is equivalent to mixing the signals together first and split the signal later

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Regarding claim 5, which inherit the limitations of claim 4, Takahiro et al teach applying a phase delay 16 to the oscillator output 15 and mixing the output signal of component 16 with incoming signal to produce a intermediate frequency. This is equivalent to the limitation of mixing the incoming signal with reference signal then splitting the resultant signal into two and phase delaying one of the split signals. It is well known in the art that multiplying two signals together and phase shifting the resulting signal to a specific angle is equivalent to phase shifting one of the signal to a specific angle and multiplying those signals together. It would be obvious to an ordinary skilled in the art to use the Takahiro's frequency discriminator to enhance the efficiency of the discriminator.

Regarding claim 6, which inherits the limitations of claim 5, Takahiro et al teach that output signal I of the detector 11 and the output signal Q of the detector 12 have phase difference of 90 degrees from each other (see column 3 line 6 – 8).

Regarding claim 7, which inherits the limitations of claim 5, Takahiro et al further teach the output signal I of detector 11 and the output signal Q of detector 12 are multiplied together by the multiplier 13. The output signal of the multiplier 13 represented as a voltage, function of time and phase error θ (see column 3 line 8 – 12).

Regarding claim 8, the second mixer is outputting an analog signal and the delta sigma modulator's input need to be digital inputs. It would be obvious to an ordinary skilled in the art to connect these components via an analog-to-digital converter to achieve the system compatibility.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jaison Joseph
Patent Examiner

SUPERVISORY PATENT EXAMINE

TECHNOLOGY CENTER 2600